

Appl. No. 10/709,922
Amdt. dated June 26, 2006
Reply to Office action of April 03, 2006

Amendments to the Claims:

Claims 1-17 (Cancelled)

Claim 18 (New): A multi-clock domain logic system comprising:

- 5 a first clock domain for doing logic operations according to a first clock and
generating a first logic signal, the first clock domain including:
a first delay element coupled to a test clock for delaying the test clock by a
first delay time to thereby generate a first delayed test clock;
a first multiplexer coupled to the first delayed test clock, and the first logic
10 signal or the first clock signal for outputting an output signal being the
first logic signal, the first clock signal, or the first delayed test clock
according to a control signal; and
a first flip-flop group including a plurality of flip-flops for doing a
scanning test according to the output signal of the first multiplexer;
15 and
a second clock domain for doing logic operations according to a second clock
and generating a second logic signal, the second clock domain including:
a second delay element coupled to the test clock for delaying the test clock
by a second delay time to thereby generate a second delayed test clock;
20 a second multiplexer coupled to the second delayed test clock, and the
second clock or the second logic signal for outputting an output signal
being the second clock, the second logic signal, or the second delayed
test clock according to the control signal; and
a second flip-flop group including a plurality of flip-flops for doing a
25 scanning test according to the output signal of the second multiplexer;
wherein the first delay time is longer than the second delay time.

Claim 19 (New): The multi-clock domain logic system of claim 18, wherein the second

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clock domain further comprises:

a third delay element coupled to the test clock for delaying the test clock
by a third delay time to thereby generate a third delayed test clock;
a third multiplexer coupled to the third delayed test clock, and the second
5 clock or the second logic signal for outputting an output signal being the
second clock, the second logic signal, or the third delayed test clock
according to the control signal; and
a third flip-flop group including a plurality of flip-flops for doing a
scanning test according to the output signal of the third multiplexer;
10 wherein the third delay time is different than the first delay time and the second
delay time.

Claim 20 (New): The multi-clock domain logic system of claim 19, wherein the first
clock domain further comprises:

15 a fourth multiplexer coupled to the test clock and the first clock for
outputting an output signal being the first clock or the test clock
according to the control signal; and
a fourth flip-flop group including a plurality of flip-flops for doing a
scanning test according to the output signal of the fourth multiplexer;
20 wherein the test clock is input to the fourth multiplexer without delay.

Claim 21 (New): The multi-clock domain logic system of claim 18, wherein the first and
the second delay elements respectively comprise one or more delay units, and
the number of the delay unit(s) of the first element is different from the number
25 of the delay unit(s) of the second element.